APPENDIX E - Jitter Definition and Related Terminologies

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Definitions

1) Jitter

High frequency deviation from the ideal timing of an event. Jitter is a period/frequency displacement of a signal from its ideal location. These displacements can occur in amplitude, phase, and pulse width and are generally categorized as either deterministic or random.

2) Correlated (deterministic/systematic) Jitter

Sum of Duty Cycle Distortion (DCD) and Data Dependent Jitter (DDJ). Jitter is based on real and repeatable direct measurements. Deterministic jitter itself may be broken into two major components - those based on the accuracy of the duty cycle of the information and those based on interaction of the 1's and 0's due to the limited bandwidth of the transmission system.

Deterministic jitter are those timing variations that are repeatable within a system and whose cause can generally be directly attributable to specific physical components or events. An example of this would be the jitter caused by the frequency selective attenuation and phase delay of a signal in a transmission line.

3) Non-Correlated (Random) Jitter

The probabilistic jitter created by random or Gaussian noise effects (shot, thermal, 1/f, etc.). Random jitter components are *rms* summed together. The ratio of peak-to-peak to rms equivalent random jitter is a factor determined by Gaussian probability of error, that is, the desired bit-error ratio. For example:

BER = 2.5E-10

Random jitter is that portion of jitter that is not repetitive in nature and is caused by external or internal noise in a system (thermal noise, EMI, etc.) This jitter is not directly predictable. It is measured by using a data pattern free of DDJ (i.e., the same pattern used to measure DCD) relative to the transmitter clock. Averaging is turned off, but infinite persistence is enabled.

4) Period Jitter

Variation in the output clock period. Important because it causes short clock cycles that reduce timing margins in synchronous circuits such as processors, reference to PLL, the period jitter is the worst case period deviation from ideal that will ever occur on the output of the PLL. The period jitter will represent an upper bound to the cycle to cycle jitter.

5) Cycle to Cycle Jitter

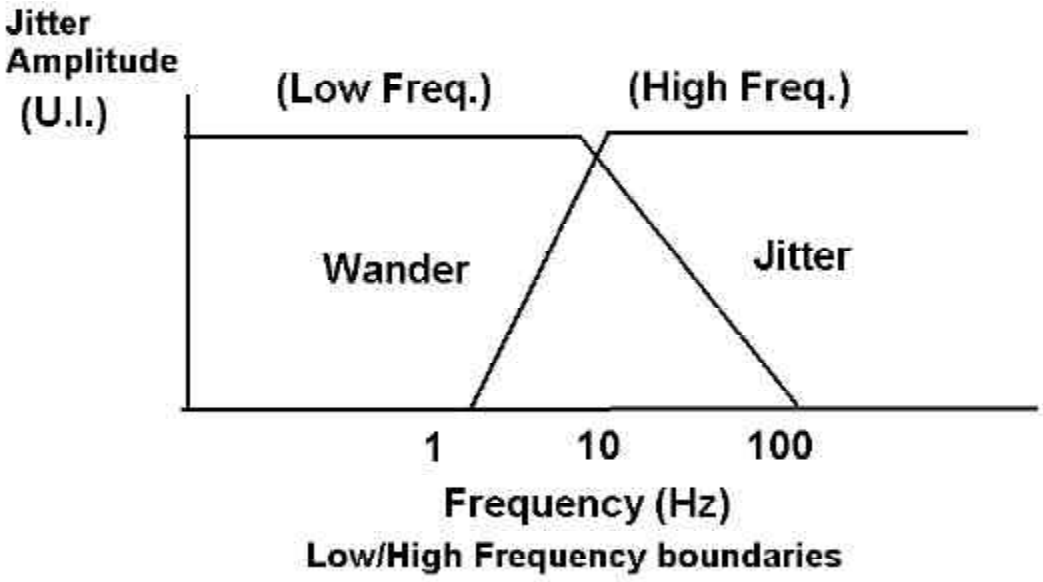
The deviation between periods of two adjacent cycles, i.e. variation of period N relative to period N-1. Because cycle to cycle jitter is defined as two adjacent periods this number is typically the smallest jitter that can be specified.

6) Long term (Accumulated) Jitter

The displacement of clock edges relative to an ideal clock over more than one cycle.

7) Low Frequency Jitter (Wander)

Jitter induced by frequency modulation below 10Hz.



Low/High Frequency boundaries

8) High Frequency Jitter

Jitter induced by frequency modulation above 10Hz.

9) Jitter Spectrum

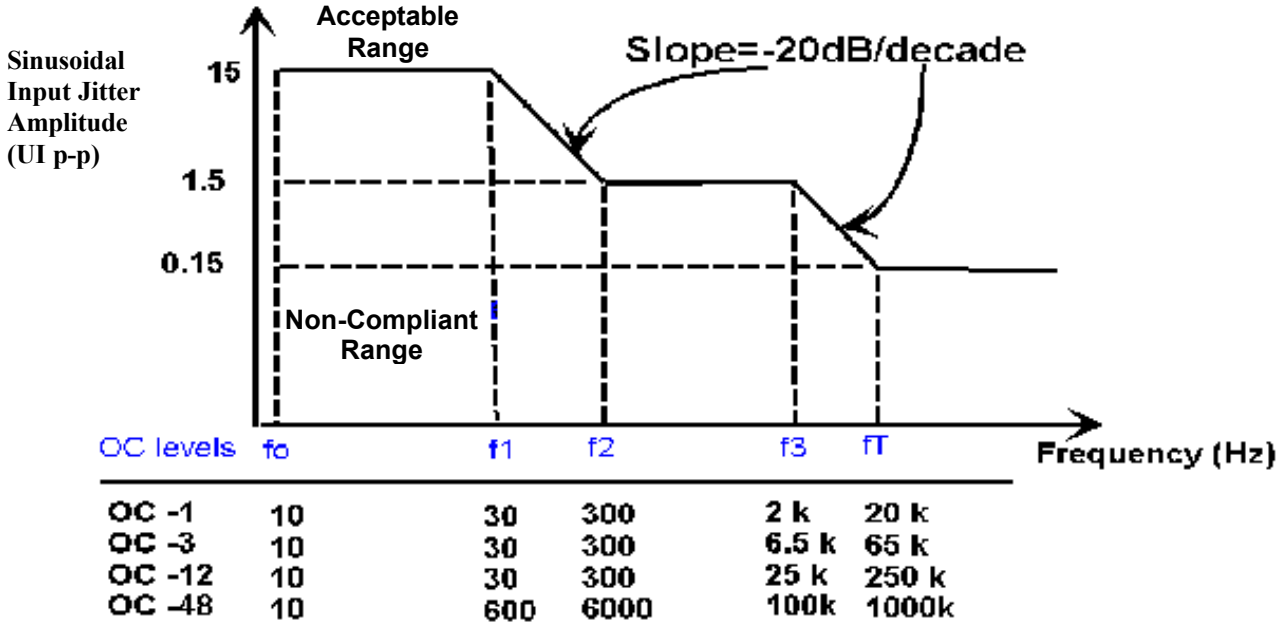
A FFT spectrum representation of Time Domain data which allows the frequency components of jitter to be displayed.

10) Input to Output Jitter

Variation in the delay from reference clock to output clock. Important when two more PLL clocks are cascaded in the system because it causes timing skew between the PLL clock outputs.

11) Jitter Tolerance

The amount of jitter that a receiver must accept and still recover data within a specified BER. Peak to peak time amplitude of sinusoidal jitter applied to the input data before output data pattern errors are observed in the recovered data. Expressed in Unit Interval peak to peak
(UIp-p), a UI is nominally one bit clock period.



SONET
Jitter Tolerance Limits

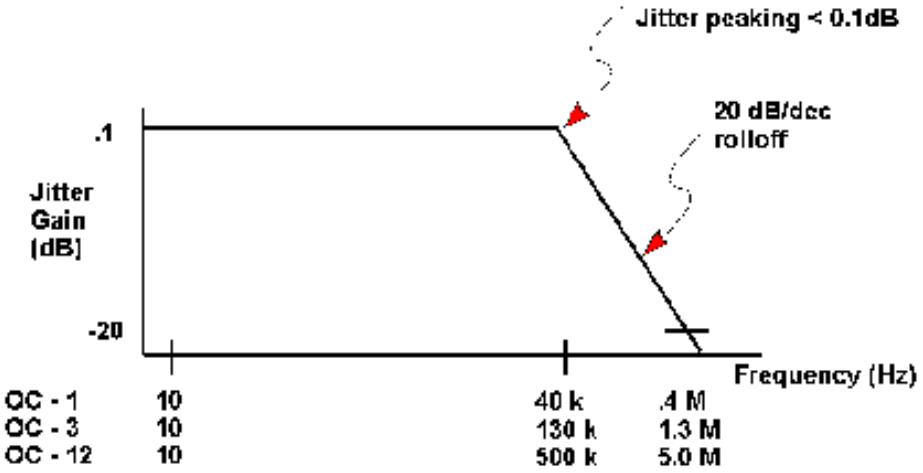
12) Jitter Generation

Generated jitter is caused by or added to a serial bit stream by a driver. Generated jitter measurements tell how much jitter is added to the data stream by sources such as inter-symbol interference, finite pulse width, pattern effects and clock-threshold offset. Described as a portion of Unit Interval (Ul) and limited to maximum 0.01 Ul for SONET using a 12kHz high pass filter. For common OC levels and data rates the following are SONET Jitter Generation Specifications.

OC level	Data Rate	Jitter Generation
OC-3	155 Mbits/sec	64ps
OC-12	622 Mbits/sec	16ps
OC-24	1.2 Gbits/sec	8ps
OC-48	2.4 Gbits/sec	4ps

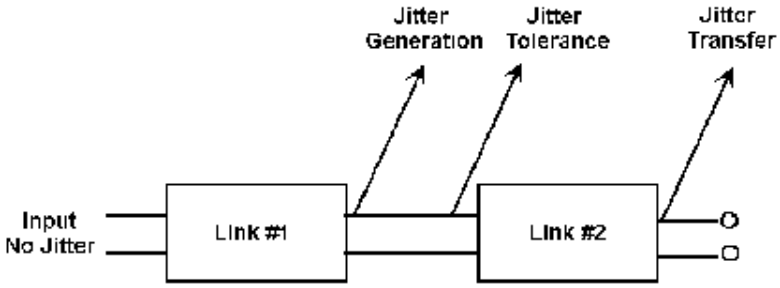
13) Jitter Transfer

Defined as the ratio of output data time jitter to the applied input data time jitter versus jitter frequency. Ratio is generally expressed in decibels [20 log (ratio)]



Jitter Transfer (SONET)
Bellcore GR-253-CORE

Jitter Accumulation



Random Jitter (RJ)

$$\text{Total Jitter} = \sqrt{(\text{Link \#1 jitter})^2 - (\text{Link \#2 jitter})^2}$$

Data Dependent Jitter (DDJ)

Total Jitter = Link #1 jitter Link #2 jitter

*DDJ increases linearly whereas RJ increases as root sum squared

14) Data Dependent Jitter

The time variation of data transition edges as caused by the length of time the prior state existed before changing states. This is from the subtle effects of saturation or cutoff time in electronic circuits. This effect contributes Intersymbol Interference, ISI, due to the attempt by prior bit to overlap into an adjacent bit interval, especially if the state interval approaches the state transition time.

DDJ is a measurement of intersymbol interference based on the maximum timing deviations caused by a worst-case data pattern. DDJ is affected by many environmental characteristics, in addition to the code used. These include the length of the cable, the integrity of the signal launched into the cable, and how well the cable is terminated.

15) Duty Cycle Distortion Jitter

Duty Cycle Distortion, or pulse-width distortion, is the difference in propagation delay time between the low-to-high and high-to-low delay times expressed in time units, or as a percentage of time relative to the original pulse duration time.

DCD manifests itself as either differences in the rise and fall times or differences in period for bits sent as a 0 compared to bits sent as a 1. DCD jitter alters the placement of all transitions in the data stream by about the same amount (in alternating directions), regardless of the bit pattern being sent. This is measured by sending a pattern down a communications link that does not exhibit DDJ and using an averaging mode on the oscilloscope to filter out any random jitter (RJ) that may be present.

16) Intersymbol Interference (ISI)

ISI is caused by short term storage effects in digital circuits. At any time, the received signal represents not only the current digital value but also the residues of previous digital values (determined by the system's impulse response). With random digital signals, the residuals appear on the eye diagram, rather like thermal noise. However, the levels are not random but are determined by the preceding digital pattern.

17) Bit Error Ratio (BER)

The bit error ratio, sometimes referred to as the bit error rate, is defined as the number of bits received in error divided by the total number of bits transmitted in a specified time interval. Within the specified interval, it is numerically equal to the bit error probability.

18) Eye Diagram

A method for assessing deterministic jitter. Typically obtained on an oscilloscope by writing all possible received sequences on top of each other while triggering the oscilloscope timebase from the data clock.